AMENDMENT TO THE CLAIMS

Claim 1 (Currently Amended): A method of driving a liquid crystal display panel of a dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines and a plurality of gate lines in a matrix array, comprising the steps of:

supplying the data lines with (n-2)th data corresponding to the liquid crystal cells connected to an (n-2)th gate line, wherein n is an integer greater than 2;

supplying a first gate start pulse;

in response to the first gate start pulse, conducting a first data supplying channel for the liquid crystal cells connected to an nth gate line such that the (n-2)th data is supplied to the liquid crystal cells connected to the nth gate line;

supplying a second gate start pulse;

in response to the second gate start pulse, conducting a second data supplying channel for the liquid crystal cells connected to the (n-2)th gate line such that the (n-2)th data is supplied to the liquid crystal cells connected to the (n-2)th gate line,

wherein conducting the first data supplying channel and conducting the second data supplying channel are performed substantially simultaneously, wherein the first and second gate start pulses are output from a pre-charging controller;

wherein the pre-charging controller includes;

a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of a data driving integrated circuit;

first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE);

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and

a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses;

wherein the liquid crystal cells connected to only first and second gate lines of the plurality of gate lines are supplied with active data signal after the liquid crystal cells connected to only the first and second gate lines were charged in advance with data signal at every frame with data signal applied at a blanking interval.

Claim 2 (Canceled).

Claim 3 (Currently Amended): The method according to claim [[2]]1, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of [[an]] the active data signal.

Claim 4 (Currently Amended): The method according to claim [[2]]1, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

Claim 5 (Currently Amended): A driving apparatus for a liquid crystal display panel of dot inversion system having liquid crystal cells arranged at intersections between a plurality of data lines and a plurality of gate lines in a matrix array, comprising: a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel;

a gate driving integrated circuit responsive to first and second gate start pulses to sequentially drive the gate lines of the liquid crystal display panel;

a pre-charging controller to generate the first and second gate start pulses to supply an (n-2)th data corresponding to liquid crystal cells connected to an (n-2)th gate line to both liquid crystal cells connected to an nth gate line and liquid crystal cells connected to the (n-2)th gate line, wherein n is an integer greater than 2;

wherein the pre-charging controller includes;

a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of the data driving integrated circuit;

first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE);

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and

a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses;

wherein the liquid crystal cells connected to only first and second gate lines of the plurality of gate lines are supplied with active data signal after the liquid crystal cells connected to only the first and second gate lines were charged in advance with data signal at every frame with data signal applied at a blanking interval.

Claims 6-7 (Canceled).

Claim 8 (Currently Amended): The apparatus according to claim [[7]]5, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of [[an]] the active data signal.

Claim 9 (Currently Amended): The apparatus according to claim [[7]]5, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

Claim 10 (Currently Amended): A device for driving a liquid crystal display panel having a plurality of data lines, a plurality of gate lines orthogonal to the plurality of data lines, and a plurality of liquid crystal cells, comprising: a data driving integrated circuit supplying data to the data lines;

a gate driving integrated circuit responsive to first and second gate start pulses to drive the gate lines;

a pre-charging controller to generate the first and second gate start pulses to the gate driving integrated circuit, wherein an (n-2)th data corresponding to liquid crystal cells connected to an (n-2)th gate line is supplied to liquid crystal cells connected to an nth gate line, wherein n is an integer greater than or equal to 2;

wherein the pre-charging controller;

a first input line supplied with a pre-gate start pulse and a second input line supplied with a data enable signal for controlling data output of the data driving integrated circuit;

first delay means for delaying the pre-gate start pulse from the first input line by one clock interval of the data enable signal in response to a data output enable clock (DOE);

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal in response to a data output enable clock (DOE); and

a gate device for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay means to continuously output the first and second gate start pulses;

wherein the liquid crystal cells connected to only first and second gate lines of the plurality of gate lines are supplied with active data signal after the liquid crystal cells connected to only the first and second gate lines were charged in advance with data signal at every frame with data signal applied at a blanking interval.

Claim 11 (Canceled).

Claim 12 (Currently Amended): The apparatus according to claim 10, wherein polarity inversion of the data signals applied to the liquid crystal cells connected to the first and second gate lines is made in at least two clock time intervals prior to an application of [[an]] the active data signal.

Claim 13 (Original): The apparatus according to claim 10, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines are applied in at least two clock time intervals before the gate and data control signals become effective data.

Claim 14 (Original): The apparatus according to claim 10, wherein the (n-2)th data is also supplied to liquid crystal cells connected to the (n-2)th gate line.

Claims 15-23 (Canceled).